Interval Arithmetic on the Cell Processor

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The Cell processor is a new processor [2], designed by IBM, Sony and Toshiba, with an innovative architecture based on 8 Synergistic Processor Elements on the same chip. Each SPE contains a synergetic processing unit (SPU), a local memory (256KB of memory for the code and the data) and a memory flow controller. The SPU [1] is composed of a 4-way SIMD single precision FPU (SpSPU) and a 1-way SIMD double precision (DpSPU). Today, the peak rate is around 200 Gflops. Each SpSPU can perform 25.6 GFlops whereas DpSPU can only do 1.8GFlops. But SpSPU has only the rounding mode toward zero and no underflow and overflow whereas the DpSPU is fully IEEE 754 compliant.

In order to deal efficiently with interval arithmetic [3] with only rounding mode toward zero, we discuss different ways to represent intervals and compare them on the SpSPU and on the DpSPU.

References:

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