A Parallel Compensated Horner Scheme

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The Compensated Horner Scheme [1, 2] is an accurate and fast algorithm to evaluate univariate polynomials in floating-point arithmetic. The accuracy of the computed result is similar to the one given by the Horner scheme computed in twice the working precision. The implementation of the Compensated Horner Scheme runs at least as fast as existing implementations of Horner Scheme producing the same output accuracy.

It is based on the so-called *error-free transformations*. These are algorithms that make it possible to compute (in pure floating-point arithmetic) the rounding error for the elementary operations (addition, subtraction and multiplication). Indeed, it is possible to show that these elementary rounding errors can be represented exactly as floating-point numbers (unless underflow or overflow occurs).

Parallelizing compensated algorithms is tedious even for summation and dot product algorithms [3]. In this talk, we will present a parallel version of the Compensated Horner Scheme. Some experiments on multicore and Graphics Processor Units (GPU) architectures will be presented to show the efficiency of this algorithm.

References

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[3] N. Yamanaka, T. Ogita, S. M. Rump, and S. Oishi. A parallel algorithm for accurate dot product. *Parallel Comput.*, 34(6-8):392–410, 2008.